UCIe 2.0 Specification: Advancing an open ecosystem for on-package chiplet innovation

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Agenda

- Introduction
- UCIe 2.0 Overview
- Introducing UCIe-3D
- Addressing SIP Challenges through DFx
- Optional Manageability Features & UDA
- Additional Updates

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Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplet Development

Guiding principles of UCIe

- Open chiplet ecosystem
- Backward compatible evolution to ensure investment protection
- Optimized power, performance, and cost metrics applicable across the entire compute continuum
- Continuously innovate to meet the needs of evolving ecosystem

Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.

High-bandwidth, Low-latency, Power-efficient, Cost-effective Interconnects for AI, HPC, Cloud, Edge, Enterprise, 5G, Automotive, Handhelds

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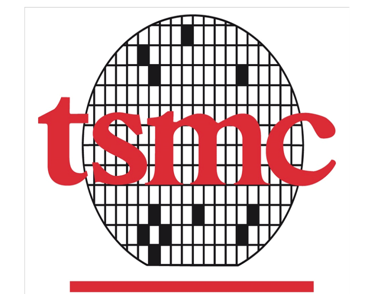
Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive the open chiplet ecosystem.



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130+ Member Companies…and growing!

- Achronix Semiconductor Corp
- Advanced Micro Devices
- Advanced Semiconductor Engineering, Inc.
- Advantest America, Inc.
- Akrostar Technology Co., Ltd
- Alchip Technologies, Ltd. Taiwan Branch
- Alibaba Inc.
- Alphawave Semi
- Amkor Technology, Inc.
- Ampere Computing
- Analog Devices Incorporated
- AP Memory Technology Corporation
- Applied Materials, Inc.
- Arm Limited
- Arteris, Inc.
- ASMedia Technology Inc.
- Astera Labs
- Atron (Chongqing) Technologies, Limited
- Ayar Labs
- Beijing Henghuizhixun Technology Co., Ltd.
- Blue Cheetah Analog Design Inc.
- BMW of North America LLC
- Broadcom Inc.
- Cadence Design Systems Inc.
- Ceremorphic, Inc.
- ChangXin Memory Technologies, Inc.
- Ciena Corporation
- CoMira Solutions Inc
- Credo Semiconductor, Inc
- Deca Technologies, Inc.
- DENSO Corporation
- d-Matrix
- Douyin Vision Co., Ltd
- Dream Chip Technologies GmbH
- DreamBig Semiconductor Inc.
- ECARX Limited
- Egis Technology Inc.
- e-Infochips Inc (An Arrow Company)
- Eliyan Corp.
- Ericsson AB
- eTopus Technology Inc.
- EVAS Intelligence Co., Ltd.
- EXTOLL GmbH
- ForwardEdge ASIC
- FuriosaAi
- Futurewei Technologies, Inc.
- Global Unichip Corporation (GUC)
- GlobalFoundries U.S. Inc.
- GM Global Technology Operations LLC
- Google
- HANA Micron, Inc.
- Honda Motor Co., Ltd.
- Huixi Technology Co. Ltd (Rhino Auto)
- IBM
- Imec vzw
- Infineon Technologies AG
- InfiniLink Inc.
- Innosilicon Microelectronics (Wuhan) Co. LTD.
- Inpsytech,Inc.
- Intel Corporation
- JCET Group Co., Ltd.
- Kandou Bus SA
- Keysight Technologies
- Kiwimoore (Shanghai) Semiconductor Co., Ltd_
- KNiulink Semiconductor Ltd.
- Kyocera-AVX
- LG Electronics
- Lightmatter
- M SQUARE Ltd. Shanghai
- M2 Semiconductor Ltd.
- Macronix International Co., Ltd
- Marvell Asia PTE Ltd
- MediaTek Inc.
- Mercedes-Benz Research & Development North America, Inc.
- Meta Platforms, Inc.
- Microchip Technology Inc.
- Micron Technology Inc
- Microsoft
- MIPS Tech LLC
- MIRISE Technologies Corporation
- Mixel, Inc.
- MosChip Technologies
- National Institute of Advanced Industrial Science and Technology
- nepes Corporation
- Neuchips Inc.
- Neuron IP Inc
- NHanced Semiconductors, Inc.
- Nippon Telegraph and Telephone Corporation
- Nissan Motor Co., Ltd.
- Nokia Solutions and Networks Oy
- Nuclei System Technology Co., Ltd
- NVIDIA
- OPENEDGES Technology. Inc.
- Physim Electronics Technology Co., LTD
- Powerchip Semiconductor Manufacturing Corp (PSMC)
- proteanTecs, LTD.
- Qualcomm, Inc.
- Qualitas Semiconductor
- Rapidus Corporation
- Rebellions
- Renesas Electronics Corporation
- Robert Bosch GmbH
- Rohde & Schwarz GmbH & Co. KG
- Samsung Electronics Co, Ltd.
- Sanechips Technology Co., LTD
- Semitronix Corporation
- Shanghai UniVista Industrial Software Group Co., Ltd.
- Shanghai Zhaoxin Semiconductor Co., Ltd.
- Shinko Electric Industries Co., LTD.
- Siemens Industry Software Inc.
- SiliconAuto B.V.
- Siliconware Precision Industries Co. Ltd.
- SK Hynix Inc.
- SkyeChip
- SmartDV Technologies
- Socionext Inc.
- Synopsys Inc
- Taiwan Semiconductor Manufacturing Co., Ltd.
- Tektronix Inc
- Tenstorrent Inc.
- Teradyne, inc.
- Texas Institute for Electronics, The University of Texas at Austin
- Texas Instruments Incorporated
- The MathWorks, Inc.
- Thine Electronics, Inc.
- Tongfu Microelectronics Co., Ltd
- Toyota Motor Corporation
- Truechip Solutions PVT LTD
- Tsavorite Scalable Intelligence, Inc
- Unisoc (Shanghai) Technologies Co., Ltd
- University of New Hampshire
- Untether AI
- Valens Semiconductor
- Ventana Micro Systems Inc
- VeriSilicon, Inc.
- VIA NEXT Technologies, Inc.
- Volkswagen Aktiengesellschaft
- Winbond Electronics Corporation
- xFusion Digital Technologies Co., Ltd
- Xi'an UniIC Semiconductors Co.,Ltd.
- Xpeedic Co., Ltd.
- Xsight Labs Ltd.
- Zero ASIC Corporation
- Zhejiang Zentel Memory Technology Co., Ltd.

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Member Driven Evolution

March 2022
- UCIe Consortium formed
- UCIe 1.0 Specification released

June 2022
- UCIe Consortium incorporated

August 2023
- UCIe 1.1 Specification released

August 2024
- UCIe 2.0 Specification released

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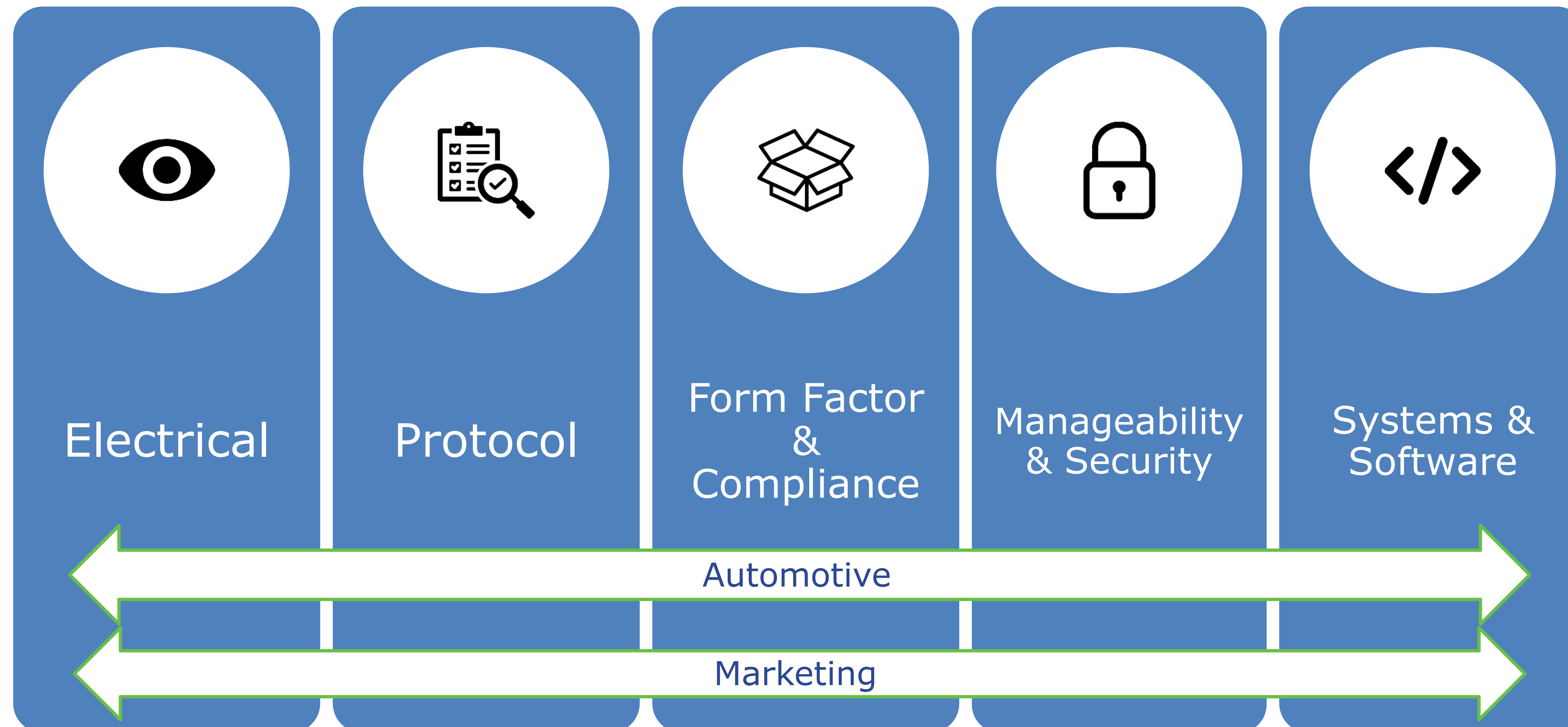
UCIe Consortium Working Groups

Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.



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UCIe 2.0 Specification Feature Overview

- Support for 3D packaging to significantly enhance bandwidth density and power efficiency
- Holistic support for manageability, debug, and testing for any System-in-Package (SiP) construction with multiple chiplets
- Ball map optimizations
- Heterogeneous package designs for interoperability and compliance testing
- Fully backward compatible with UCIe 1.1 and UCIe 1.0

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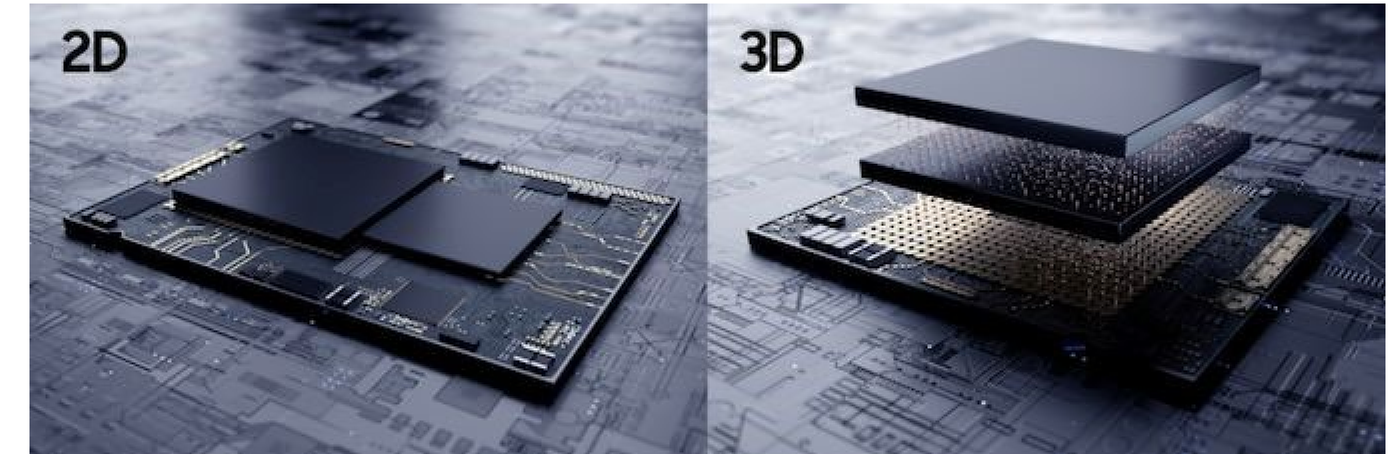
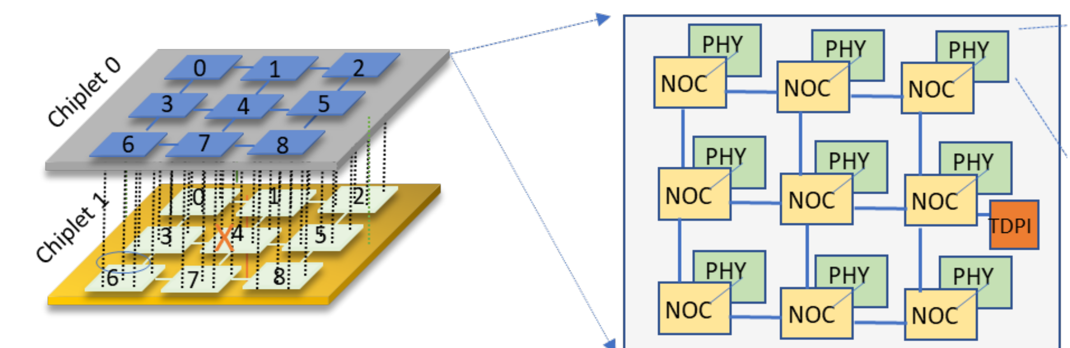
UCIe-3D for Vertical Integration

- Evolution from UCIe 1.0/1.1 to UCIe 2.0 with 3D chiplets
- Bump pitch scaling and bandwidth density benefits
  - Optimized for <=10 um bump pitch with >10 to 25um also supported
  - Significant increase in # of connections (inversely squared with area)
  - 3D interconnect reduces interconnect distance between chiplets to practically 0
- Areal connection advantages and PHY area utilization
  - Not limited to sides = entire chiplet area available





Example Usage (Figure 5, UCIe 2.0 Specification)

- Increased bandwidth density and reduced bump pitch
- Simplified associated circuitry for bump-limited design
- Power efficiency gains with reduced interconnect distance

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Expanding Industry Leading KPIs to 3D

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments for UCIe 3D
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Up to 4	= SoC Logic frequency – power efficiency is critical
Width (each cluster)	16	64	80	Options or reduced width to 70, 60…
Bump Pitch (µm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe-3D fits within the bump area, must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	FtF bonding initially; FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224	165 – 1317	N/A (vertical)	
BW Density (GB/s/mm^2)	22 – 125	188 – 1350	4000 at 9µm	4TB/s/mm^2 @ 9µm, ~12TB/s/mm^2 @ 5µm, ~35TB/s/mm^2 @ 3µm, ~300TB/s/mm^2 @ 1 µm
Power Efficiency Target (pJ/b)	0.5	0.25	<0.05 at 9µm	Conservatively estimated at 9µm pitch <0.02 for 3µm pitch
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	BER < 1E-27
ESD	30V CDM		5V CDM → ≤ 3V	5V CDM at introduction, no ESD for W2W hybrid bonding possible

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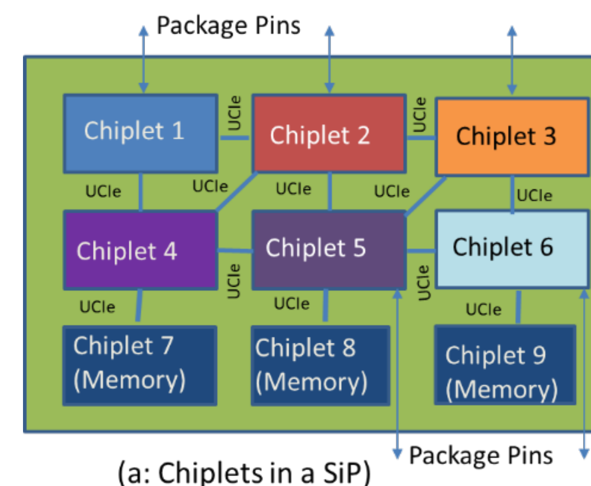
Design for Manageability and Test/Debug/Telemetry (DFx)

- Support at chiplet and SiP level to manage and test in a plug and play ecosystem
  - Examples: lane margining, compliance testing, fault reporting, sideband access
  - Different chiplets could have different interfaces or supported speeds
  - Only access control security is defined in UCIe 2.0.

- Throughout the Si life cycle: From the die at sort, to package/bond, to field level debug or repair

- UCIe 2.0 defines:
  - Common infrastructure using current IP building blocks as well as external interfaces at the package level
  - Bridging to connect to an external interface (e.g., SMBus or PCIe) for off-package connectivity.
  - Root of Trust

- UCIe 2.0 manageability may be used to perform services such as:
  - Discovery of chiplets and their configuration
  - Initialization of chiplet structures and parameters
  - Error reporting
  - Retrieval of log and crash dump information
  - Test and debug
  - Aspects of chiplet security



(a: Chiplets in a SiP)

Test/Debug Interface	Bandwidth
UCIe-S	Main band: 512Gb/s/direction [x16 @ 32Gb/s] Side band: 800Mb/s/direction
PCIe	1024Gb/s/direction [x16 @ 64Gb/s]
USB	80 Gb/s/direction [x2 @ 40Gb/s]
JTAG (IEEE 1149.1)	5-100Mb/s/direction
IEEE 1838	>100Mb/s/direction with FPP
I2C/SMBus	400Kb/s
I3C	33Mb/s/direction

(b: Bandwidth of various Interfaces: UCIe and External)

Source: UCIe 2.0 Whitepaper Fig 1
1b) references interfaces that can be probed, e.g. UCIe bumps

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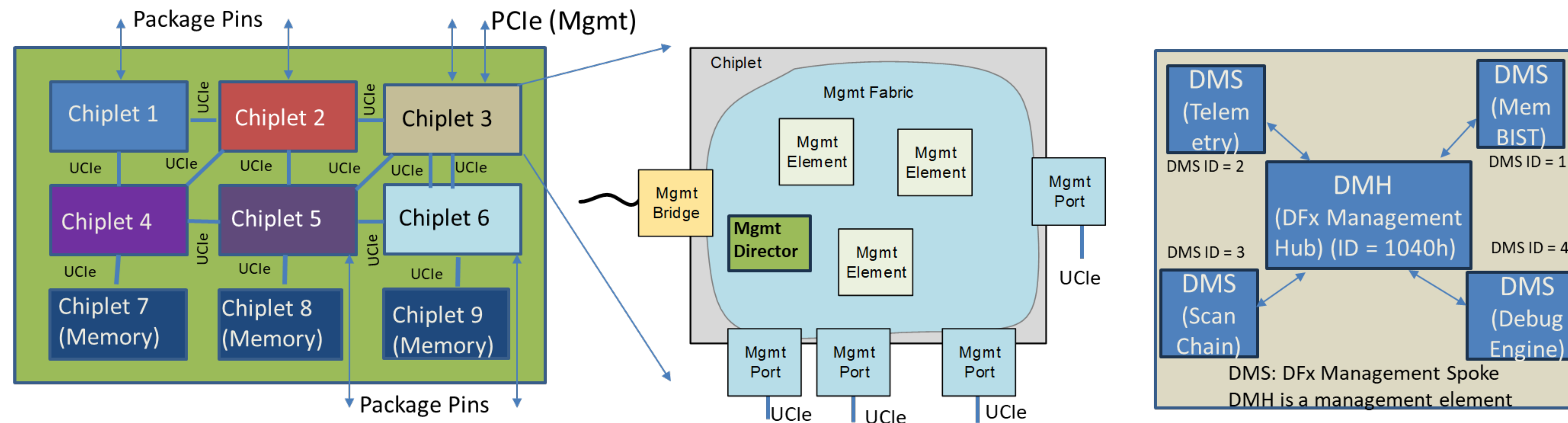
UCIe DFx Architecture (UDA)



- Hub-Spoke model within each chiplet
- Each chiplet supports a DFx Management Hub (DMH): gateway to accessing all test, debug, and telemetry capabilities within a chiplet
- DMH provides discovery and routing of management transport packets to various DFx Management “Spokes” (DMS)
- Spokes are the entities implementing a given test, debug, or telemetry functionality
- Config registers + UCIe-wrapper on top of existing registers provide a common framework for software
- Vendor-specific drivers can be loaded for each unique functionality, based on the Device ID (DID) of the spoke

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Summary

- UCIe Consortium continues to evolve UCIe technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and towards a robust compliance mechanism.

- UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.
  - Tremendous support across the industry with several companies announcing IP/VIP availability
  - Evolving as *the* interconnect of SoCs just as PCIe and CXL at the board level
  - UCIe 2.0 Specification is available to the public https://www.uciexpress.org/specification

- UCIe Consortium welcomes interested companies and institutions to join the organization at the Contributor or Adopter level.

- 6 Technical Working Groups (Electrical, Protocol, Form Factor/Compliance, Manageability/Security, Systems and Software, Automotive) alongside the Marketing Working Group are driving the technology toward the future.
  - Incredible innovation happening in the Consortium!

- Get involved! Learn more by visiting www.UCIexpress.org

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Thank You

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